

preselected voltage levels, and said output terminal coupled to deliver binary signals that vary between the first preselected voltage level and a third preselected voltage level, the third preselected voltage level different than the second preselected voltage level and determined by a voltage source coupled to the output terminal;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion coupled to a voltage supply to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal.

8. (Fourth Amendment) An apparatus for converting first digital signals that vary between a first and second preselected voltage levels to second digital signals that vary between the first and a third preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to receive said first signals, said source coupled to deliver said second signals and coupled to a voltage source which determines said third preselected voltage level to a level different than the second preselected voltage level, said gate coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and

a pump coupled to the gate of said pass gate transistor, said pump being configured to increase the voltage level applied to said gate during a transition from the first to the second preselected voltage levels.

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13. (Fourth Amendment) An apparatus for converting an input signal that varies between first and second preselected voltage levels to an output signal that varies between the first preselected voltage level and a third preselected voltage level, comprising:

63
a pass gate transistor having a gate, source, and drain, said drain coupled to receive said input signal, said source coupled to deliver said output signal and coupled to a voltage source which determines said third preselected voltage level to a level different than the second preselected voltage level, said gate coupled to a voltage supply;

a capacitor coupled across said source and drain of said pass gate transistor; and
means for increasing the voltage level applied to said gate during a transition from the first to the second preselected voltage level.

REMARKS

In the office action mailed November 1, 1999 (the present office action), claims 1-20 (all claims) are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Fox U.S. Patent No. 3,579,023, Nelson, U.S. Patent No. 4,507,618, and GB 1,2287,021. Applicant has amended claims 1, 8, and 13. The amendments add no new matter and are amply supported by the specification; see for example page 7 lines 1-8.

The office action asserts that it would be obvious to substitute a transistor for a resistor to reduce circuit size. Assuming, arguendo, that this is so, there is nonetheless no teaching or suggestion in any of the cited references to couple the input terminal of a transistor to receive binary signals, the output terminal to deliver binary signals, and to